

ABSTRACT OF THE DISCLOSURE

A system for a four-transistor random access memory cell includes a first transistor of a first conductivity type having a gate coupled to a word line and a source
5 coupled to a bit line, a second transistor of the first conductivity type having a gate coupled to a drain of the first transistor and a source coupled to receive a first voltage, a third transistor of a second conductivity type having a gate coupled to a drain of the second transistor, a
10 source coupled to receive a second voltage and a drain coupled to the drain of the first transistor, and a fourth transistor of the second type having a gate coupled to the drain of the first transistor, a source coupled to receive the second voltage and a drain coupled to the drain of the
15 second transistor. Other systems are also provided.